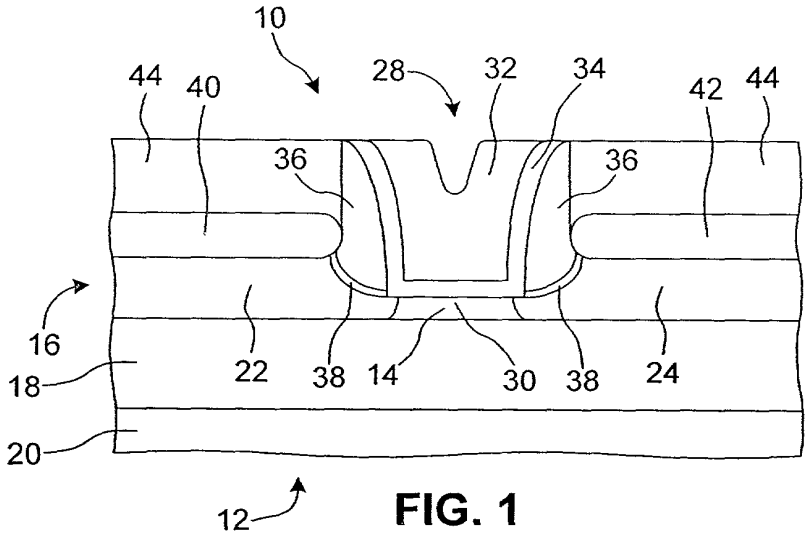
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FIG. 1

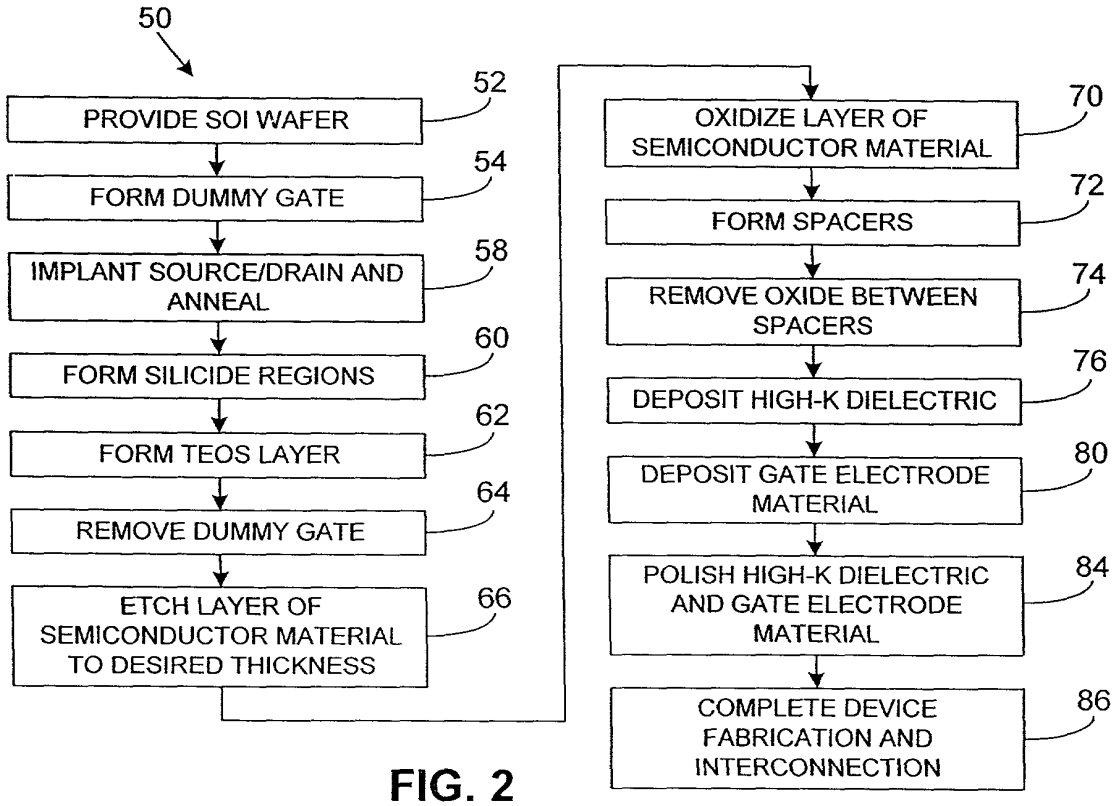
50
PROVIDE SOI WAFER
52
FORM DUMMY GATE
54
IMPLANT SOURCE/DRAIN AND ANNEAL
58
FORM SILICIDE REGIONS
60
FORM TEOS LAYER
62
REMOVE DUMMY GATE
64
ETCH LAYER OF SEMICONDUCTOR MATERIAL TO DESIRED THICKNESS
66
OXIDIZE LAYER OF SEMICONDUCTOR MATERIAL
70
FORM SPACERS
72
REMOVE OXIDE BETWEEN SPACERS
74
DEPOSIT HIGH-K DIELECTRIC
76
DEPOSIT GATE ELECTRODE MATERIAL
80
POLISH HIGH-K DIELECTRIC AND GATE ELECTRODE MATERIAL
84
COMPLETE DEVICE FABRICATION AND INTERCONNECTION
86

FIG. 2

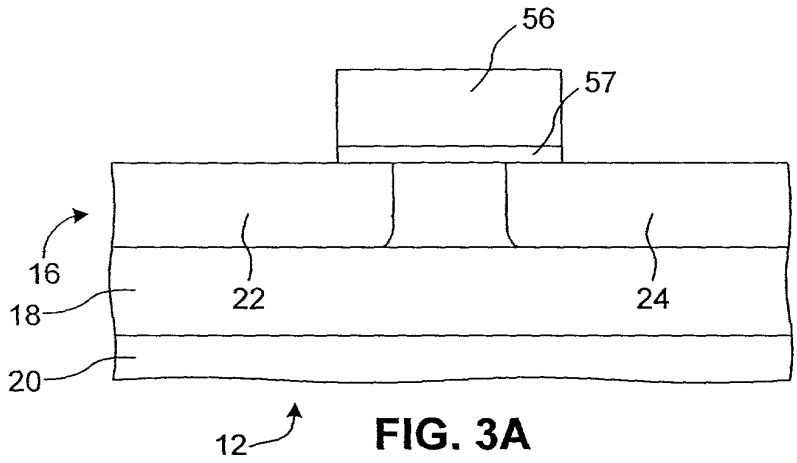

FIG. 3A

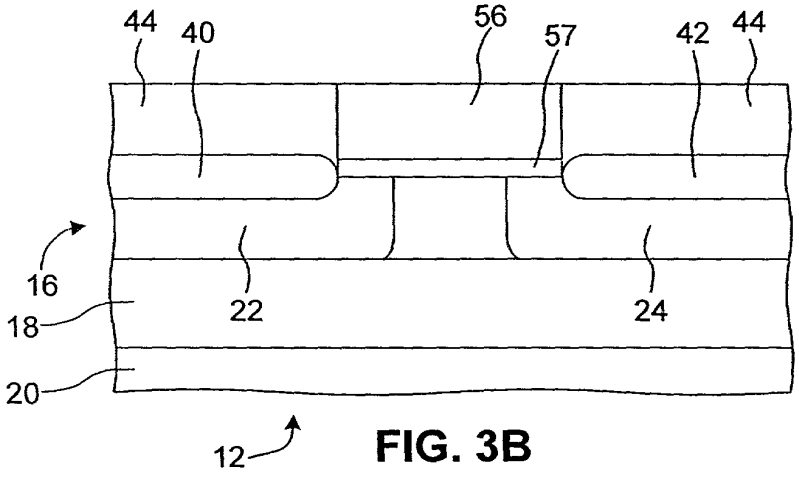

FIG. 3B

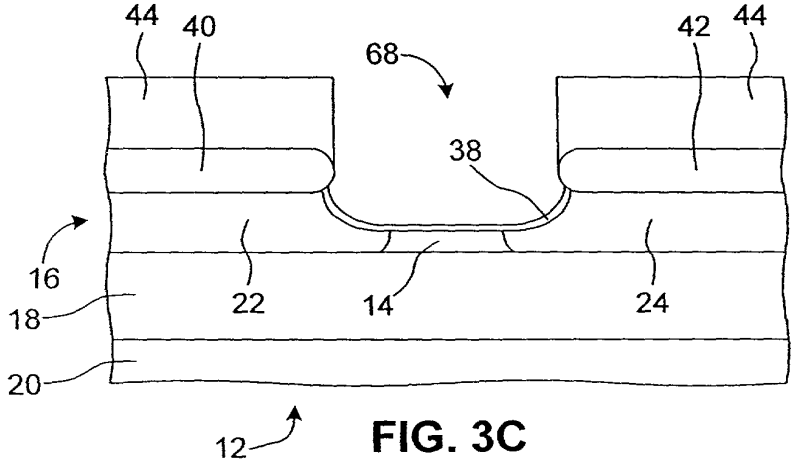

FIG. 3C

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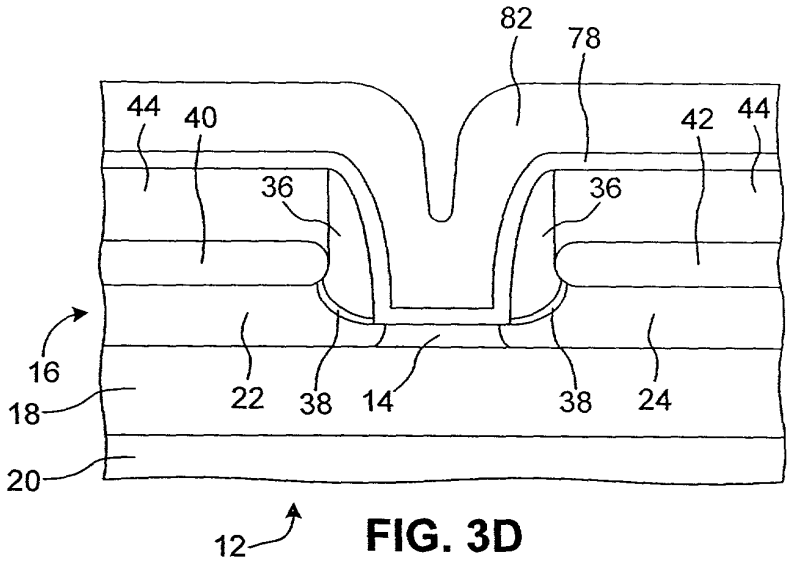

FIG. 3D

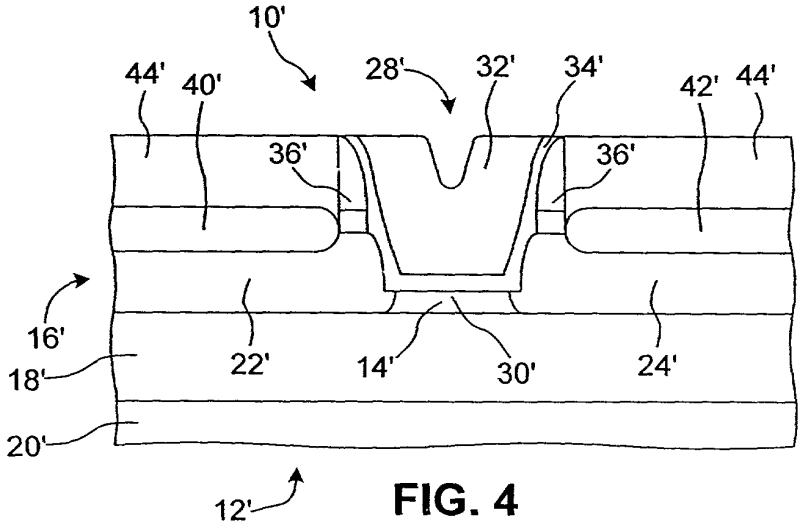

FIG. 4

EL 936 436 US